Design for Testability

Flying Probe Series 1 and Series 2 Testers

Version 3
Code : 81110142.067

SPEA

Contents

Introduction

This document is addressed to anyone involved in the design of useful and functioning boards that, at the same time, have to be easy to assemble and test. The professions usually concerned in this process are:

1) the electronic engineer
2) the pcb designer

The SPEA Flying Probes system is able to test even the boards not conceived or designed according to the "Design for Testability" standards.

Nonetheless, this document contains not binding rules and suggestions that make possible, for the designer, to test the board in the best possible way and in total freedom.
Applying these rules and suggestions during the board designing process allows getting a more complete and less expensive test.

Therefore, this document allows to drastically reduce the time and cost of the test. Designing the boards according to the parameters specified in this document generates substantial time and money savings. In addition to that, it also leads up to higher efficiency and precision of the test, as well as higher profitability of the product.

Applying the contents of the "Design for Testability" document allows to:

1. Reduce the involving of the designers during the production start-up.
2. Increase the know-how exchange and cooperation between design, engineering and production technicians.
3. Reduce the starting and normal costs of the production cycle.
4. Provide a better diagnostic for component or pin, with consequent reduction of the average repair time.

Some important concepts of this document are highlighted using the following symbols:


Economic profit, saving on the test cost.


Time profit during the test program development.


Reference to SPEA documents providing detailed information.

Symbols and abbreviations:

- FP: Flying Probes
- UUT: Unit under test
- TPGM: Test program
- RSL: Removable Shuttle Loader
- OBP: On Board Programming
- PCB: Printed circuit
- "●" on tables: Supported or present
- "-" on tables: Not supported or not present

1. General aspects of board design

1.1. Mechanical design of the board

The Flying Probe (FP) systems are able to accept different kind of boards. The mechanical characteristics of the board (UUT), although within the limits described in the system datasheet, can positively or negatively influence the time of the debug and, consequently, the overall cost of the application. The FP can fly over or work around the components without particular limitations and reach the contact points at different heights. This allows a huge versatility of use with different kind of boards. It is possible to touch even the pin of a connector, for instance to test its continuity with the printed circuit.
The system datasheet reports data about the maximum board characteristics manageable by the FP systems, sorted by system model.

Design a panel of board taking a profit of the maximum system test area available on own system decrease the operator time.

Keeping all of the contact points at the same height reduces the test program developing time and consequently the cost of test.

Mounting components lower than 55mm allows to use the standard test systems, without need for the Extra Height option.

Reducing as much as possible the total components higher than 7mm gives to the probes more opportunities to make contact, thus reducing the test program developing time. The consequent reduction of the test time increases the productivity.

By concentrating the components higher than 7mm on a particular area of the board, and consequently keeping the components lower than 7mm away from them, creates befits in terms of accessibility and test program development process.

The speed of the FP depend of the pads dimension to be contact. Design the pads with the maximum dimension allowed to decrease the testing time and relative developing cost.

Please refer to the datasheets of the single systems for detailed information.

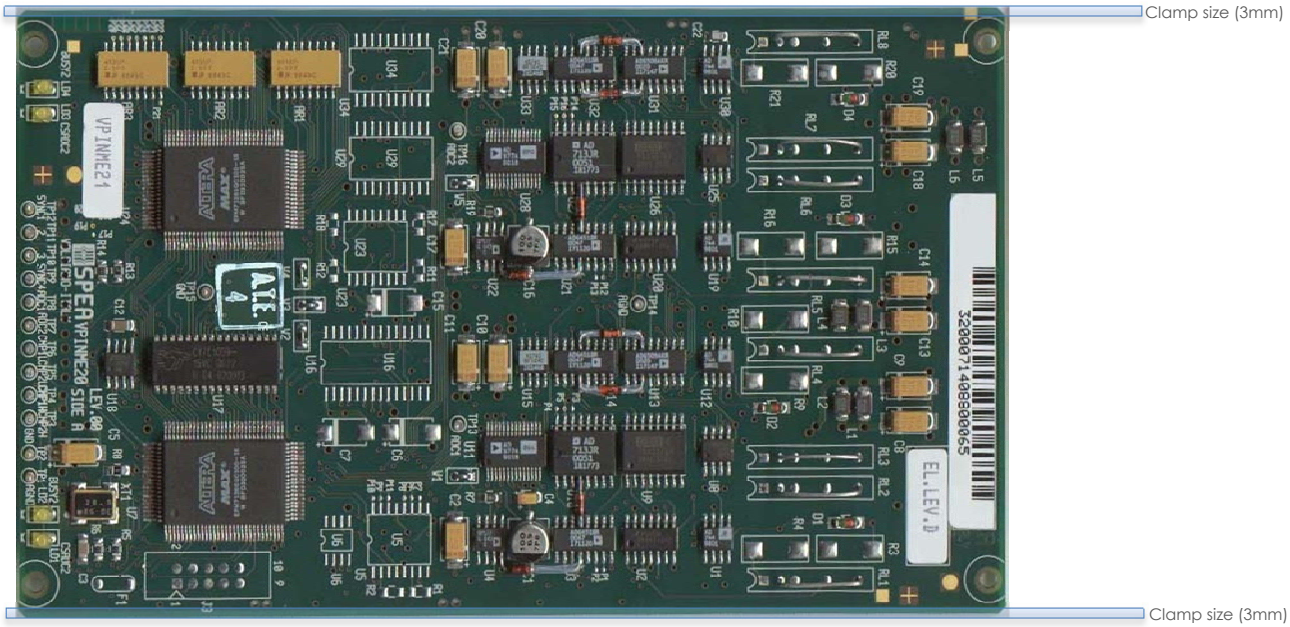


Fig. 1.1.a – UUT, top view.

Arranging a clamp area large enough can save the cost of manufacturing the transport pallet eventually needed (whether it is created during the PCB designing or as a fixture for the test program).

Refer to the system datasheet in order to know all mechanical parameters of the Uut manageable by the Flying Probes tester model to use (weight, components height, dimension, …).

1.2. Fiducials

1.2.1. Main Features

A fiducial is any component on the print circuit board with an unambiguous and repeatable shape, placed at the same coordinates on each board. The FP employs a camera vision system, which allows it to detect the fiducials and find them on the board, working the same way as the "pick and place" assembly machines. Detecting the fiducials is essential to identify the board inside the test area, compensating eventual inaccuracies in positioning and non-orthogonalities. Even if the FP is able to use any point with repeatable, unambiguous shape and placed at the same coordinates, arranging the fiducials since the designing phase leads up to a series of benefits during the program development and following tests.

Main suitable characteristics for fiducial design	**Benefits for the Test Program developer**	**Economic benefit**
Designed on CAD	The SPEA software detects and automatically uses the fiducial	Less time needed to develop the Test Program
Not tin-plated	Learning one model is enough to detect it consistently	Less time needed to start up the Test Program in production
Surrounding area free of copper traces or screen-printed signs	Less restrictions to the area involved in the detection of the fiducial	The increased repeatability means shorter overall test time
Surrounding area free of similar components	No need to choose as a fiducial another point not designed for this function	Less time needed to develop the Test Program and start it up in production
(Asymmetrically) placed on the corners of the board	No need to choose as a fiducial another point not designed for this function. If the points are asymmetrical, the system will be able to detect a board flipped by 180° and skip the test.	The more the fiducial is placed on an external position, the higher is the accuracy of the orthogonal correction. Consequently, the increased repeatability on the point of contact means less time for the test program execution.
Placed both on top and of bottom of the board	The SPEA software detects and automatically uses the fiducial	Less time needed to develop the Test Program

1.2.2. Shape

The FP is able to learn fiducials of any shape. Nonetheless, respecting specific characteristics may simplify the job of the operator in developing the test program.

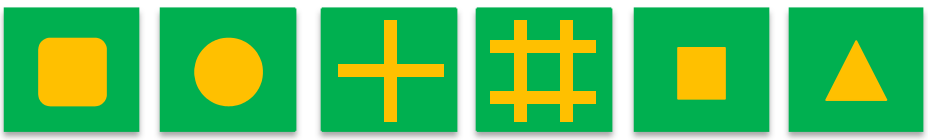


Fig. 1.2.2.a – Examples of suggested fiducials.

Independently by the chosen fiducial, avoiding the tin-plating during the production enhances the repeatability of the detection. The shape of tin-plated fiducials may vary from board to board, thus increasing the start-up time.

A point specifically designed to be a fiducial offers better repeatability which means shorter test time. All of this brings to higher overall productivity.

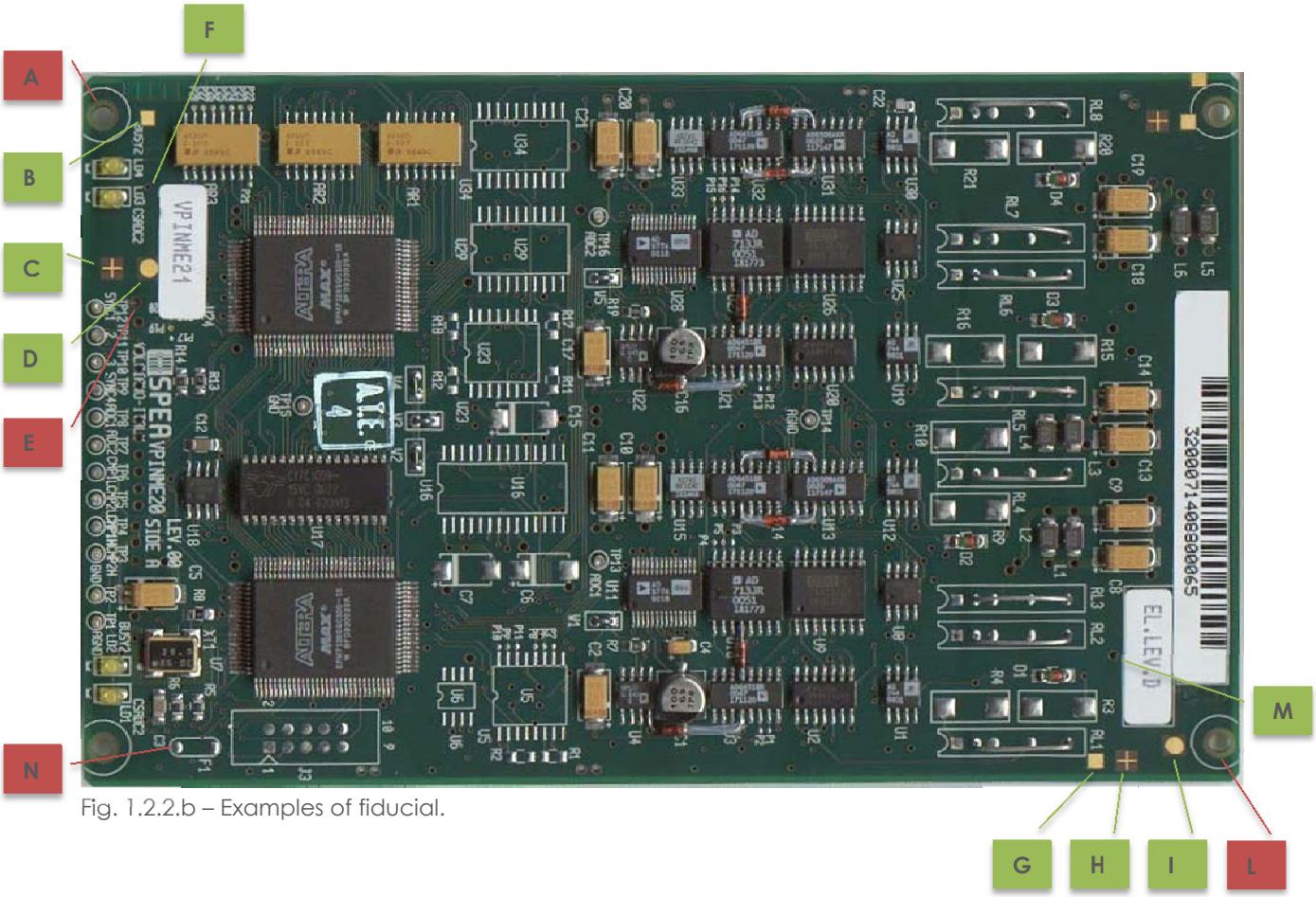


Fig. 1.2.2.b – Examples of fiducial.

	Type	Repeatability	Recommended
A, L	Mechanical hole	Low	No
B, C, D, G, H, I	(Not tin-plated) gold-plated component	High	Yes
N	Tin-plated pads or pins	Low	No
E	VIA, surrounded by similar holes	Low	No
F, M	VIA, not surrounded by similar holes	High	Yes

1.2.3. Fiducials on panels of boards

On panel of boards, the FP system is able to save on the overall test time by using panel fiducials. It is possible to use two specifically designed fiducial placed on the edge of the panel (C-D in Fig. 1.2.3.a) or two points on the boards, asymmetrical from one another (es. A-B in Fig. 1.2.3.a); in either way, the same standard of the board fiducials must be used. For the main characteristics, refer to chapters 1.2.1 and 1.2.2.

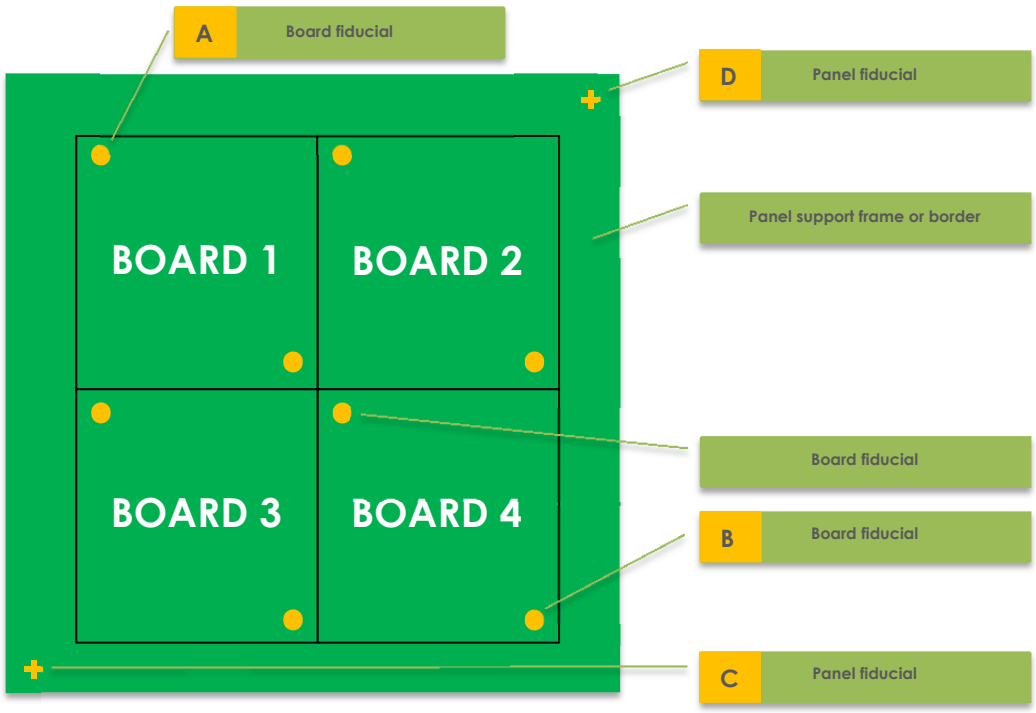


Fig. 1.2.3.a – Fiducials example on a panel of boards.

Designing the panel fiducials allows to save machine cycle time on the overall test to the benefit of productivity.

Using only two fiducials to align all of the boards of the panel allows to reduce the start-up time need by the operator that will develop the test program.

1.2.4. Fiducial for board presence check

The FP method to determine whether a board is mounted on panel and has to be tested is similar to the one used by the pick'n place machines. This is done through two types of fiducials called:

1) **General panel fiducial (All Board Mark)**
   Used to determine if 1 or more boards on the panel are not mounted.

2) **Single board fiducial (Single Board Mark)**
   Used to determine if the board is mounted or not.

Designing these two kinds of fiducials during the routing of the CAD allows to the TPGM developer on FP to identify them quickly and easily. The following table illustrates the method of the FP to use these 2 points:

	Status	Detection	Meaning	Following step
All board mark (A)	Covered	FAIL	1 or more boards are not mounted	Check the Single Board Mark
	Uncovered	PASS	All of the boards on panel are mounted	Execute the TPGM on all boards
Single board mark (B)	Covered	FAIL	The board is not mounted	The TPGM is not executed
	Uncovered	PASS	The board is mounted	Execute the TPGM on the single board

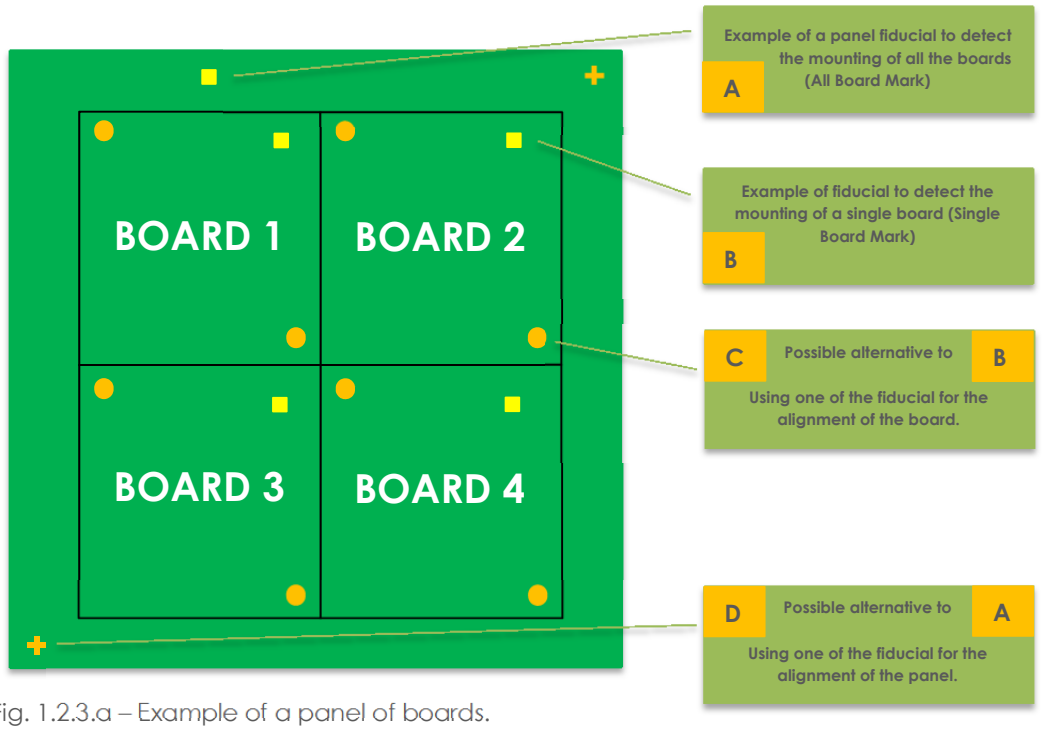


Fig. 1.2.3.a – Example of a panel of boards.

Designing fiducials to check the mounting of the boards simplifies the debug operations and saves time during the TPGM development.

1.3. Accessibility and benefits of the accessibility study

The board accessibility can be defined as the **predisposition of the board to be easily tested**.
Although the FP is able to test boards of any kind, the accessibility is a key factor during the test program realization.
An example to clarify the concept of accessibility: imagine having a Ferrari (the SPEA FP) and intending to drive at full speed in the center of Rome (your UUT); under these conditions, the Ferrari will necessarily have to adapt to the limits prescribed in the center of Rome (traffic lights, speed limits, pedestrians, ...) . It will be different if you decide to run on a racetrack, where it's possible to freely exploit the power of the Ferrari engine.
This analogy explains the following concept:

Higher accessibility = Higher performances

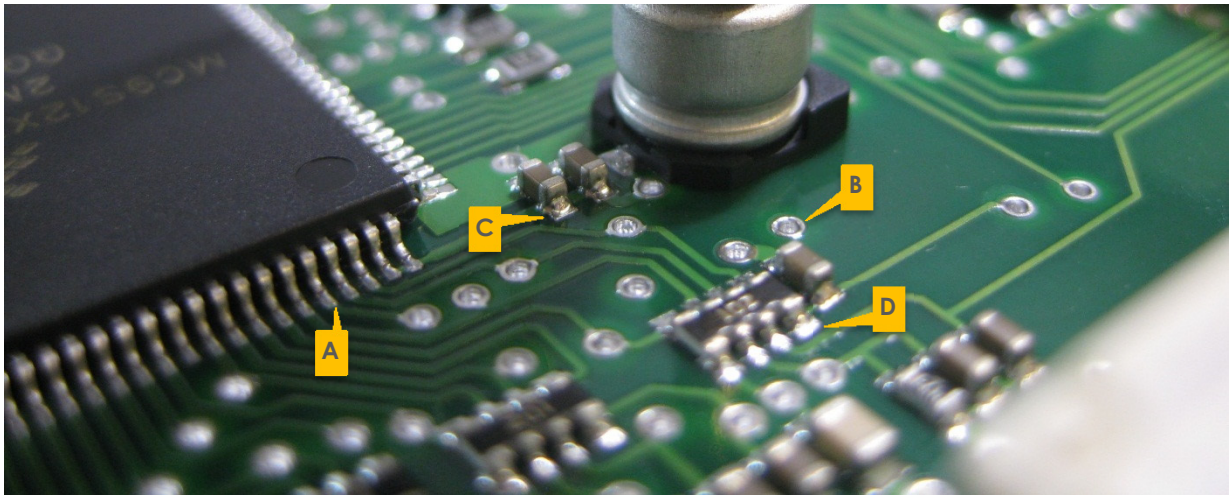


Fig. 1.3.a – Example of accessibility points.

The following table reports several examples of methods to create accessibility to the points highlighted in Fig. 1.3.a .

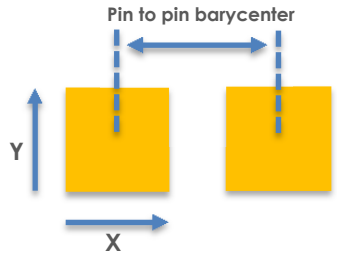
	How to create accessibility	Disadvantages of inaccessibility
A	Arrange a contact pad longer than the component's pin	In lack of a pad, touching a possibly bad mounted component could cause the probe to slip and create spurious contacts
B	Remove solder mask from via holes.	VIA holes are test points always present, stable and repeatable. If masked, it will be necessary to use alternative points, less apt to be contacted.
C	Arrange a contact pad longer than the component's length.	In lack of a pad, touching a possibly bad mounted component could cause the probe to slip and create spurious contacts
D	Arrange a contact pad longer than the component's length.	In lack of a pad, touching a possibly bad mounted component could cause the probe to slip and create spurious contacts

The following chapters explore several ways to make the board accessible in order to test it easily and in the shortest time possible.

1.3.1. Contact points on Flying Probes

The SPEA Flying Probes can touch several kinds of contact points. Nonetheless, designing the board while bearing in mind that it will be tested with flying probes can remarkably simplify the application development and its production start-up. This chapter highlights that the test with flying probes does not have any particular limit, but entails huge economic advantages if the board is prearranged to be completely or in part tested with FP.
Greater will be the size of the contact point as X-Y and better the performance in term of the FP speed will be able to offer.

	40xx S1-S2	How to identified this value for Uut design?
Minimum pin to pin barycenter	400 um	To be consider the probes used for test (refer to the Consumable catalogue).
Min contactable package	System datasheet	Refer on related system datasheet.
SMD pad contacting	•	-
TH pin contacting	•	-
VIA contacting	•	-
Ideal pad dimension	≥ 500x500 um	-
Recommended pad dimension	≥ 300x300 um	-
Minimum pad dimension	250x250 um	-
Surface requirement	Conductive	-



A "**test point**" is any point of any component (VIA, SMD, TH, Test Pad, …) which presents at least the following characteristics:

1. **Planarity**
2. **Conductivity**
3. **Minimum dimensions (see table above)**

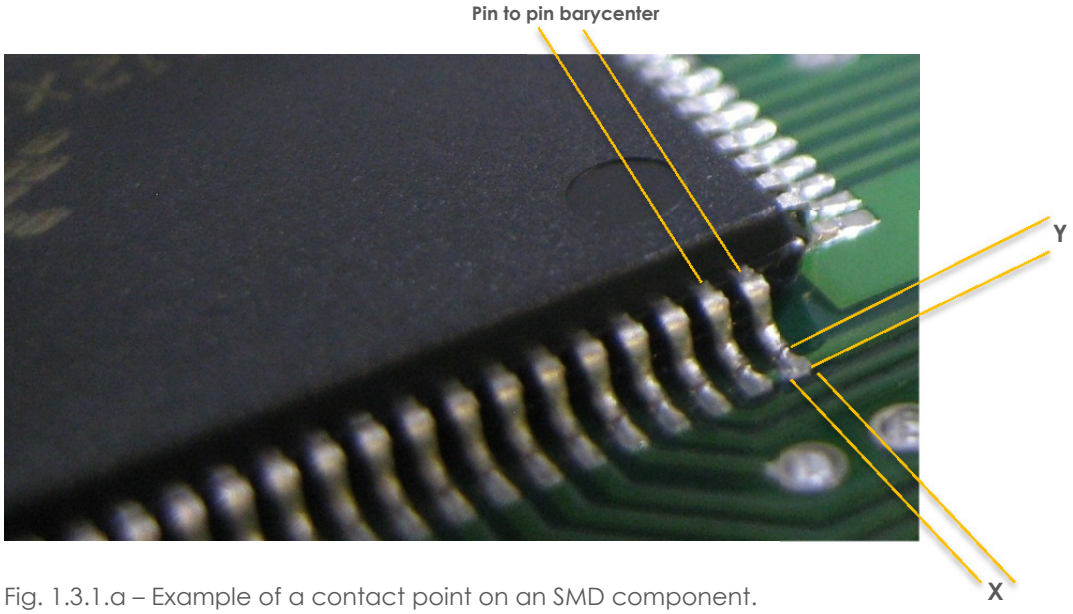
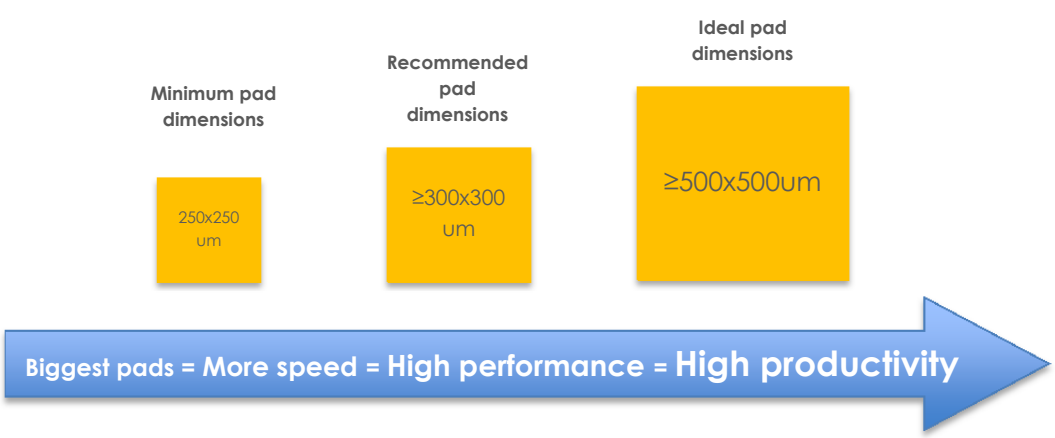


Fig. 1.3.1.a – Example of a contact point on an SMD component.



Note:

The minimum pad to be contact is dependently from the system used and from the speed it would be contacted.

Fig. 1.3.1.b – Relationship between pads dimension and test speed.

Arranging **ideal dimension** of the contact points allows to speed up the debug of the test points increasing the global productivity.

Arranging **ideal dimension** of the contact points allows to use spring probes with less performance therefore less expensive.

The general developing time and cost of the test is related to the touching pads. More is big the pad to touch and more will be the test program execution speed and development.

The number of board to be produced is a fact to be considered during the design of the contact points. Greater accessibility of the board, greater the size of the pad contact, higher will be the hourly productivity.

1.3.2. Test pad

A Test Pad is a point covered in conductive material, and it's the ideal component to use for testing, whether it is with flying probes or bed of nails. Despite that, the designing of test pads meets with limits in today's increasingly miniaturized technology when allocating space for these valuable components.

To better manage the space on the board, two kinds of Test Pads can be designed:

a) **Terminal**
b) **Embedded on track**

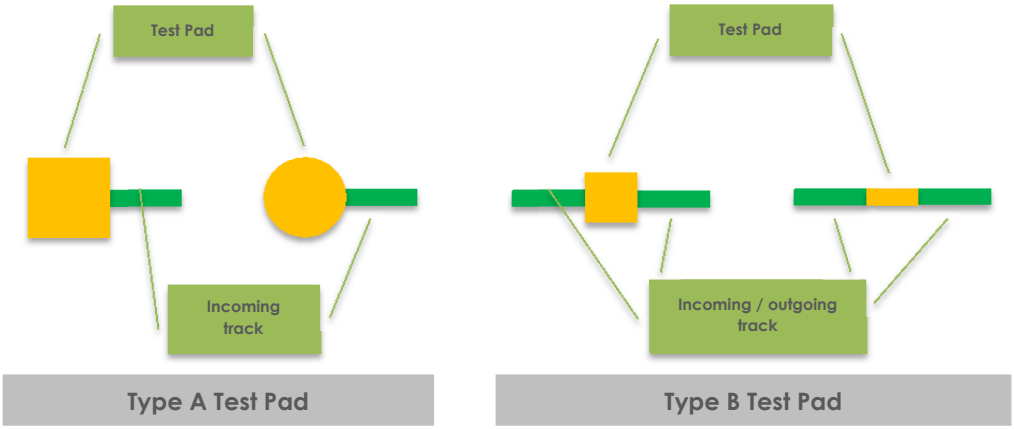


Fig. 1.3.2.a - Examples of Test Pad design

Designing pads for test allows to save time when debugging the TPGM, shortening the time needed to start up the production.

A board designed with Test Pads big enough makes possible to exploit the FP systems' top speed available, with the consequent benefits on the total test time. And that means higher productivity.

1.3.3. Via

Via is an essential component in board design that, if conveniently devised for test, can be one of the best components to use, beside the Test Pad. Unlike the Test Pad, Vias are always present on multi-layer boards. Thus, if arranged to be contactable, Vias can be invaluable allies when testing a board. To ensure the via contactability it's important that the component is not covered in non-conductive material (known as Solder Resist). Figure 1.3.2.a shows several examples of Via design.

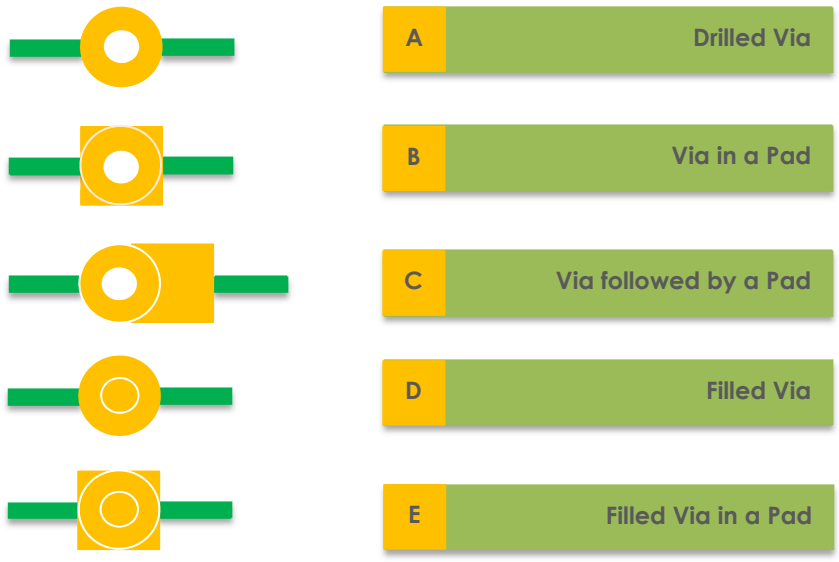


Fig. 1.3.3.a - Examples of Via design

Via typology	Notes	
A, B, C, D, E	1)	Identify each kind of Via with a different code (e.g.: **A** for Vias covered in Solder Resist, **B** for Vias not covered in Solder Resist, **C** for full Vias, **D** for drilled Vias etc.)
B, C, D, E	2)	They can be contacted out of their focal point by using spring probes other than pyramidal (which are specifically designed for Vias); consequently, Vias don't limit the choice of spring probes for the development of the application.
C, D, E	3)	They can be contacted by almost any kind of spring probe available.

Applying note no.1 can remarkably reduce the development time of the TPGM when the contact on Vias is chosen. The TPGM of a board with different kinds of Vias, not handily identified on CAD, will take considerably longer to be developed.

Applying note no.2 allows to create alternative contact points on the same Via. The TPGM developer may consider to use spring probes other than the pyramidal ones to contact Vias designed as in examples B, C, D, E.

Fig. 1.3.3.b reports some limits in using the drilled Vias with the 3 standard spring probes usually provided along with the system:

1) **Pyramidal Spring probe (devised to contact Vias)**
2) **Needle Spring probe (devised to contact Ultra-Fine Pitch devices)**
3) **4-point Crown Spring Probe (devised to contact most test points)**

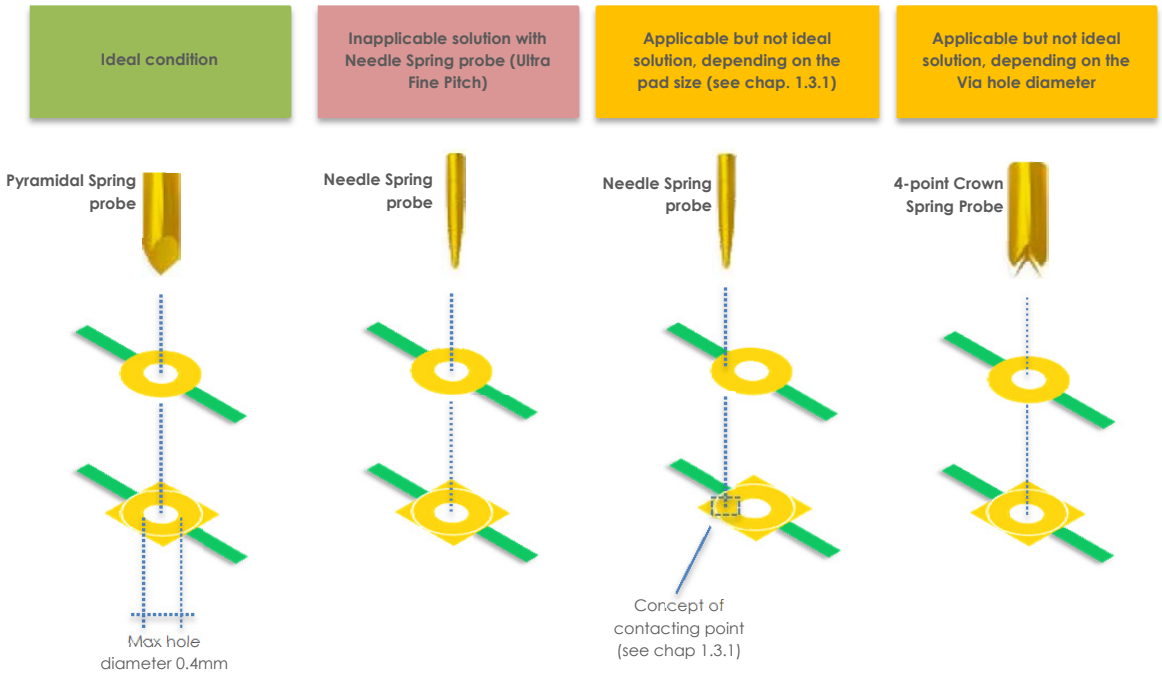


Fig. 1.3.3.b – Examples of limits of drilled Vias

1.3.4. SMD solder pads

To simplify the contacting of the FP, the best practice in designing the SMD pads is to "extend" the pad over the outline of the component to be mounted, taking into account the space occupied by the solder. Using this expedient is possible to create ideal Test Pads for the FP. Here are some examples of recommended and discouraged layouts.

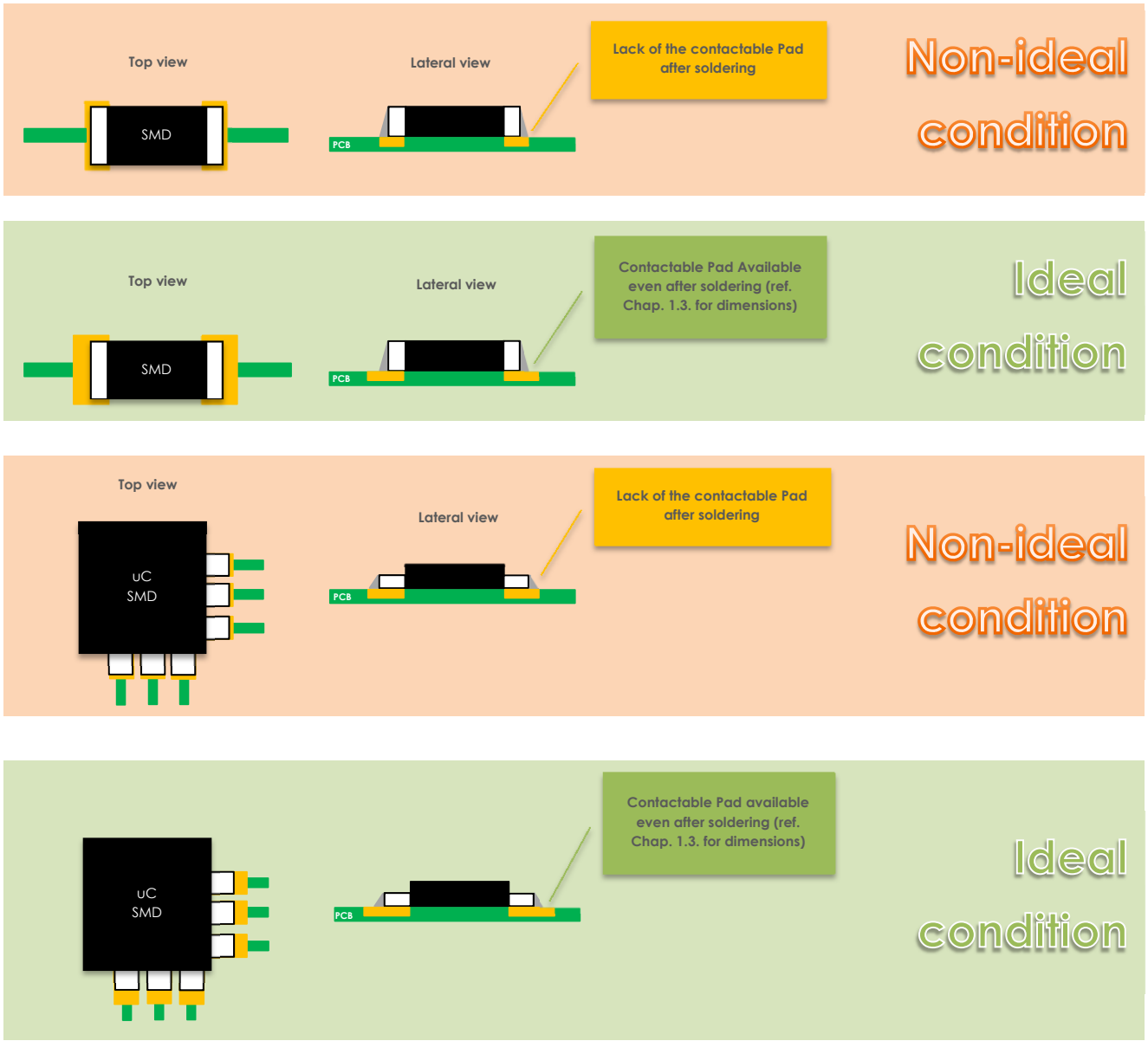


Fig. 1.3.4.a – Examples of SMD Pads

Designing "extended" SMD Pads allows to create stable and repeatable contact points that help to speed up the creation of the TPGM. The production start-up operations will be easier as well.

Arranging enough space for an ideal-sized Test Pad by extending the SMD pin allows to execute the FP programs at top speed, producing benefit in terms of throughput per hour.

1.3.5. TH traditional components

The FP doesn't suffer particular limitations in contacting this family of components since the size of the Pad to touch is usually bigger than the ideal recommended.

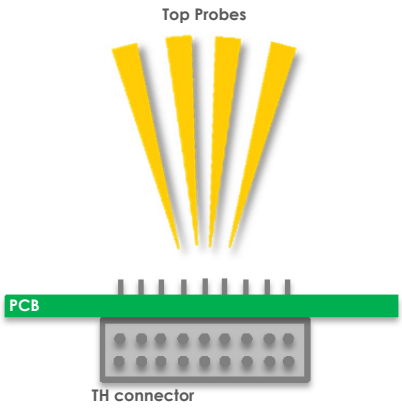


Fig. 1.3.5.a – Example of a TH connector

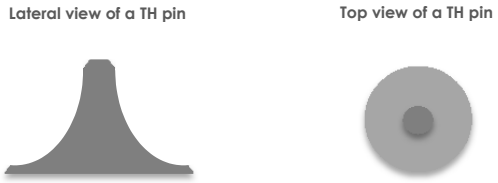


Fig. 1.3.4.b – Example of TH soldering

Using traditional TH pins allows to create stable and repeatable contact points that help to speed up the creation of the TPGM. The production start-up operations will be easier as well.

1.4. Fixturing and wiring to enhance test performance

During the board design process it is possible to arrange the use of external resources to enhance the performance of the test. The contact points that have to be touched in order to exploit those resources have to be designed ad-hoc according to the test system used. The following figure shows some typical solutions adopted in using external resources.

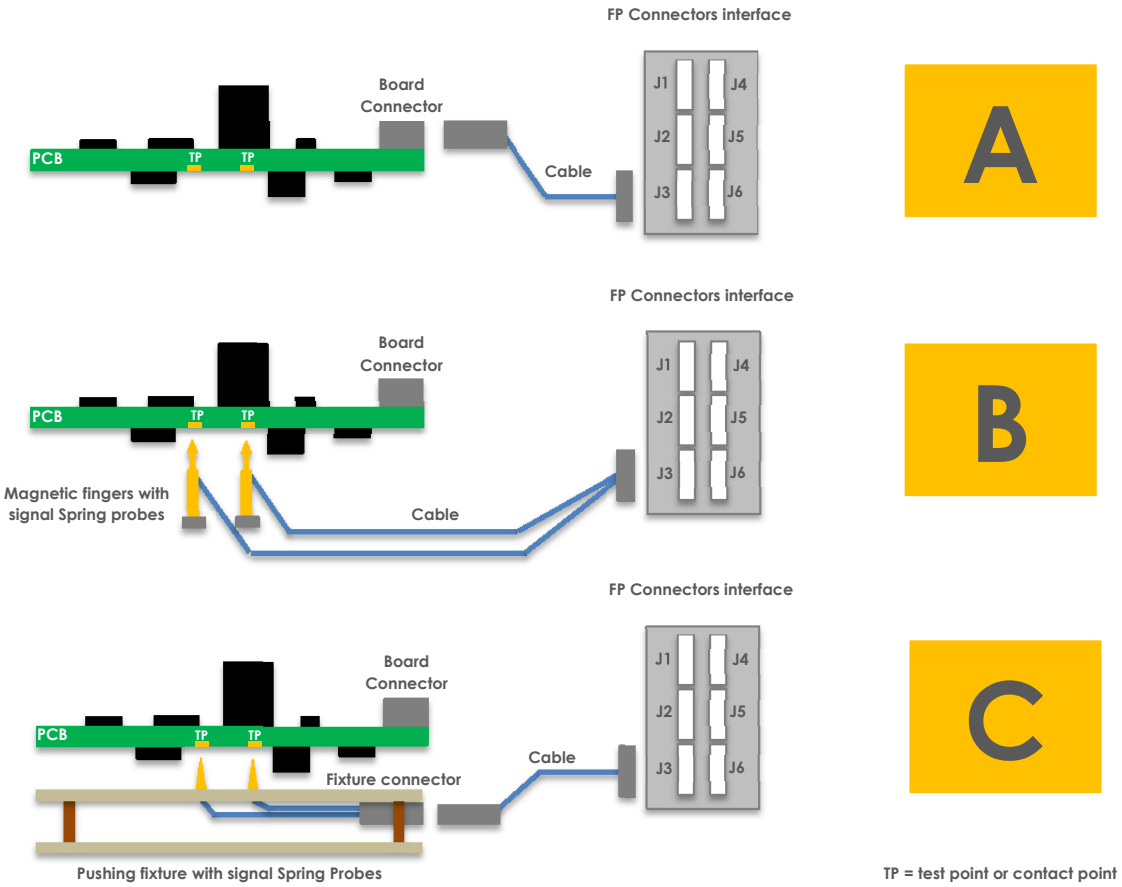


Fig. 1.4.a – Typical solutions in using external resources

The solutions vary according to several factors of different importance. If the board needs to be powered to execute the so-called "Power-On" tests, it's advisable to make so that the points to be powered can be contacted from outside using one of the three solutions above; their characteristics are summarized in the following table.

	Solution A Cabling	Solution B Fingers from the bottom side	Solution C Fixture
Applicability on In-Line systems	• (1)	-	•
Applicability on Manual systems	•	•	•
Applicability on single boards	•	•	•
Applicability on panels of boards	• (2)	• (2)	•
Contact point minimum diameter	-	1.5mm	0.8mm
Contacts distribution	-	Uniform	Uniform
Minimum ideal center to center distance between contact points	-	24mm	2.54mm (100mils)
Minimum center to center distance between contact points	-	24mm	1.27mm (50mils)
UUT tooling holes required	-	-	2
Minimum tooling holes diameter	-	-	3mm
Cost of setup	Low	Average	High
Interval of setup on system	At each test	Once, at production start-up	Once, at production start-up

(1) RSL (Removable Shuttle Loader) required
(2) To check according to the kind of test to be executed on the UUT

1.5. Irregularly-shaped boards

It is possible to test not regularly-shaped boards on FP. In order to do that, two possible solutions exist:

1) Using a special transport pallet, in epoxy glass or a similar material
2) Using magnetic pushing fingers with board clamps (where available)

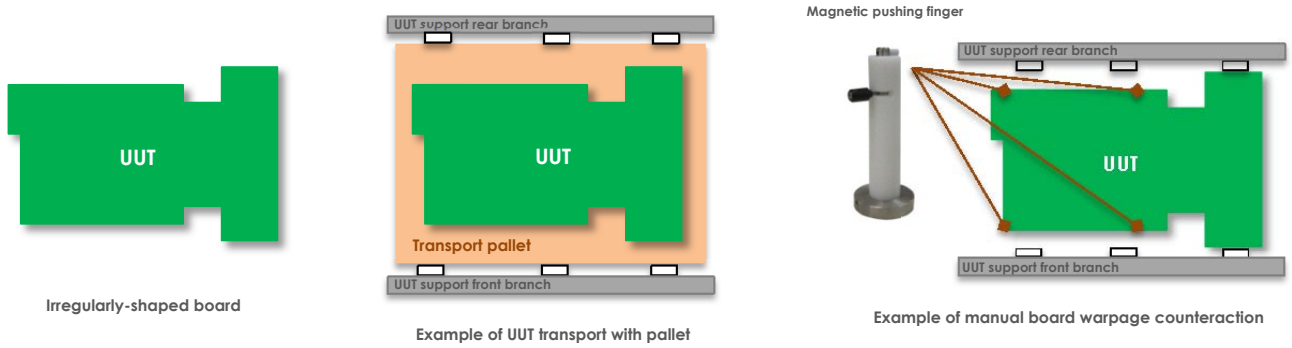


Fig. 1.5.a – Examples of transport/fixing of irregularly-shaped boards

The following table shows the applicability ranges for each method according to the system model:

	Shuttle Loader	Manual	In-Line	Back Panel
Transport pallet	•	•	•	•
Magnetic pushing fingers	•	•	• (1)	• (1)

(1) RSL (Removable Shuttle Loader) required if available on system used for testing.

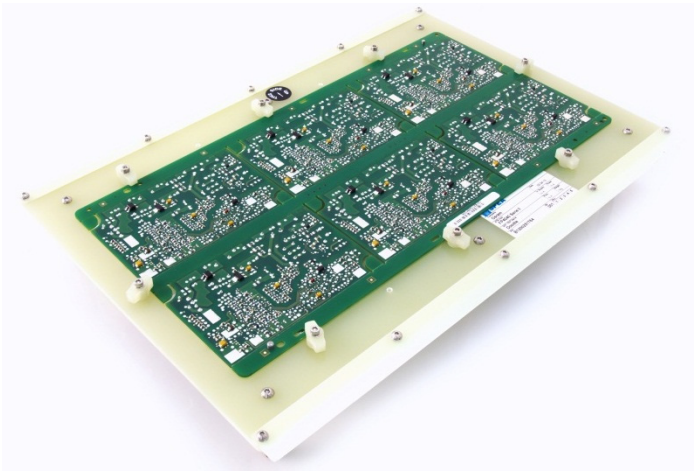


Fig. 1.5.a – Example of a transport pallet

Arranging since the designing phase a frame to give a regular shape to the UUT reduces the setup costs linked to the construction of a transport pallet or the use of magnetic pushing fingers.

The time needed to setup the test of a regularly-shaped board is notably shorter than for an irregularly-shaped one. Consequently, in the latter case the throughput per hour decreases.

1.6. Panels of boards

When designing a board, the best practice to optimize the assembly and test times is to arrange it in panels of more boards. The FP is able to manage the test on both single boards and panel of boards. The following table reports the main data:

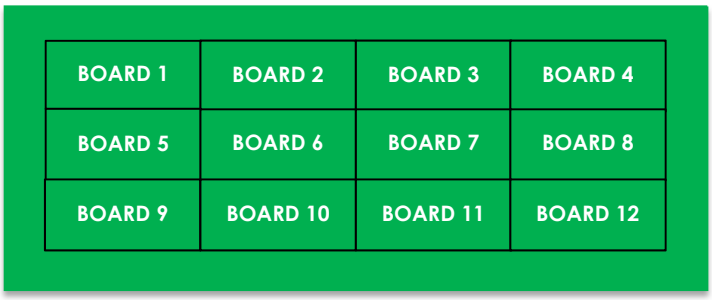


Fig. 1.6.a – Example of a panel of boards

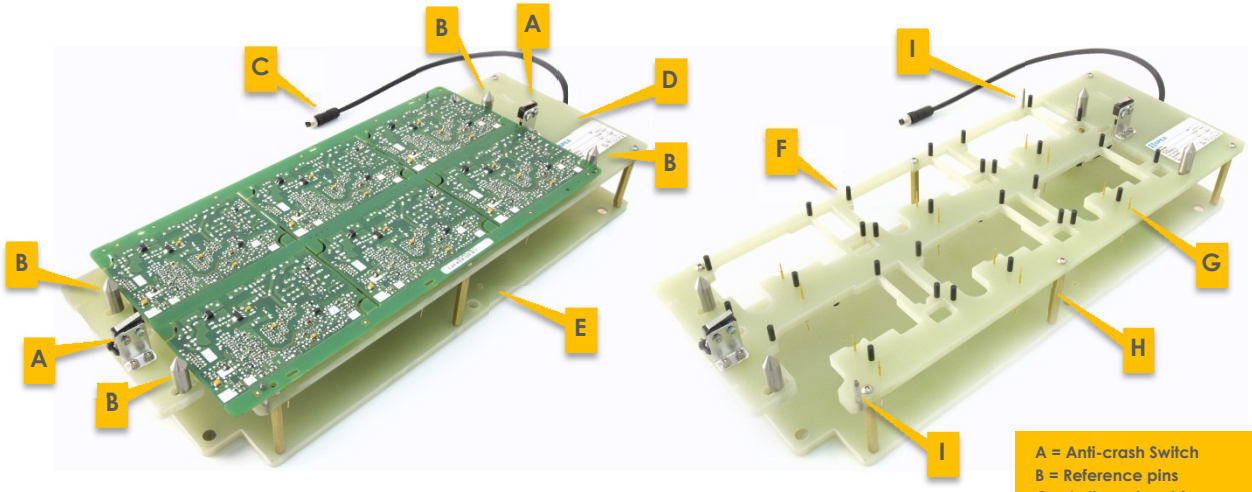
Max manageable number of boards per panel	256
Rotation management between boards	•
Top/bottom rotation management between boards (1)	•
Manageable angles of rotation between boards	0-360°
Board fiducials	Required
Panel fiducials	Optional
Single board mark for board presence check (2)	Optional
All board mark for panel presence check (2)	Optional

(1) Available through double test program (top/bottom).
(2) Refer chap. 1.2.4 for further details.

A panel of boards allows to save on the setup time compared with a single UUT. Consequently, the throughput per hour increases.

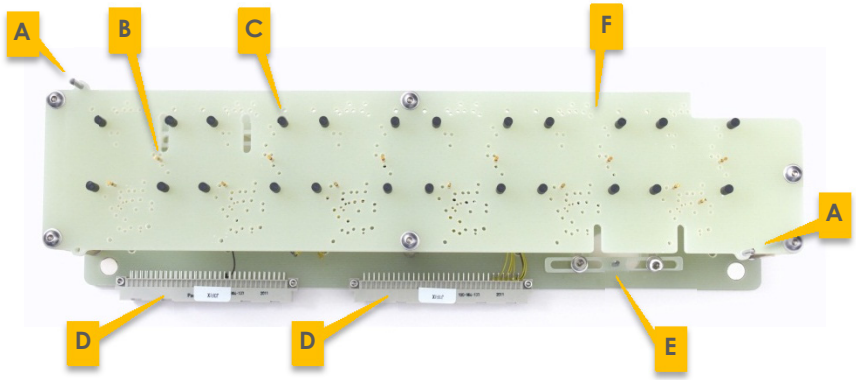
1.6.1. Fixturing on panel of boards

When designing a fixture as external hardware to enhance the test performances, it is advisable to follow some reference instructions to simplify and save money on the setup. The fixture will be manufactured to contact the UUT from the bottom using special spring probes (usually of the same kind used for Bed of Nails systems), while the FP probes will contact it from the opposite side.



A = Anti-crash Switch
B = Reference pins
C = Anti-crash cable
D = Fixture top layer
E = Fixture bottom layer
F = UUT Stand-offs
G = Signal spring probes
H = FP floor-fixture spacers
I = Centering pins

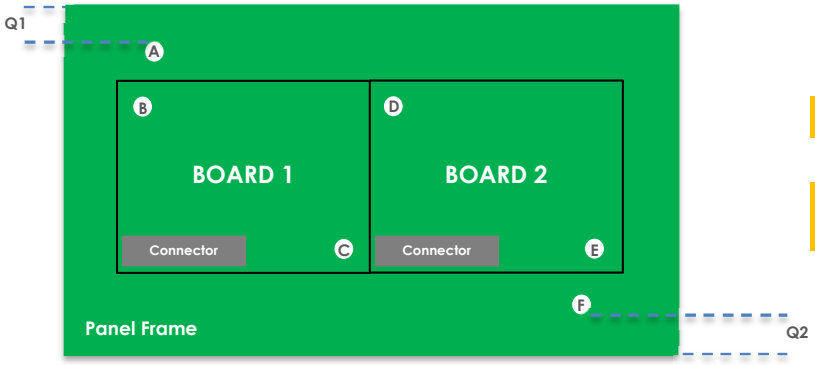
Fig. 1.6.1.a – Example of a 6-board panel fixture for an In-Line system



A = Centering pins
B = Signal spring probes
C = UUT Stand-offs
D = Feedback connector to FP interface
E = Fixture bottom layer
F = Fixture top layer

Fig. 1.6.1.b – Example of a 6-board panel fixture for a Manual system

To save money on the setup it is necessary to favor standard solutions over customizations, thus it is advisable to design the board according to a series of parameters shown in the table following Fig. 1.6.1.c.
The fixture is connected to the system through Flat type cables (in most cases) or customized cables (in particular cases).



1.6.1.c – Example of a 2-board panel to be tested using a fixture.

The table below schematizes the key points to consider when designing the board, according to the model of the system:

	Shuttle Loader	Manual	In-Line	Back Panel
Min **diameter** A, B, C, D, E, F	3mm	3mm	3mm	3mm
Minimum Q1, Q2 if used for tooling	1mm	1mm	7.5mm	7.5mm
Test points distribution on the bottom	uniform	uniform	uniform	uniform

(1) Do not concentrate the test points on a specific area of the UUT to avoid bending it with the push of the spring probes on the bottom side.

If the UUT mechanical references are suitably designed, it will be possible to save the hours of work necessary for the arranging of particular setups due to the noncompliance with the quotes specified on table.

1.6.2. Cabling on panel of boards

In particular cases, it is possible to adopt a solution with cables to enhance the test performances even if the UUT is on a panel of boards (power ON tests, functional test, etc).
All the signals needed for the test through cable have to be available on an external connector (see Fig. 1.6.2.a). This solution is not usually endorsed for several reasons such as the time needed for the setup, the space required for the cable on the boards, the necessity to disconnect the signals between boards, etc, but it's nonetheless a working alternative to manage particular situations.

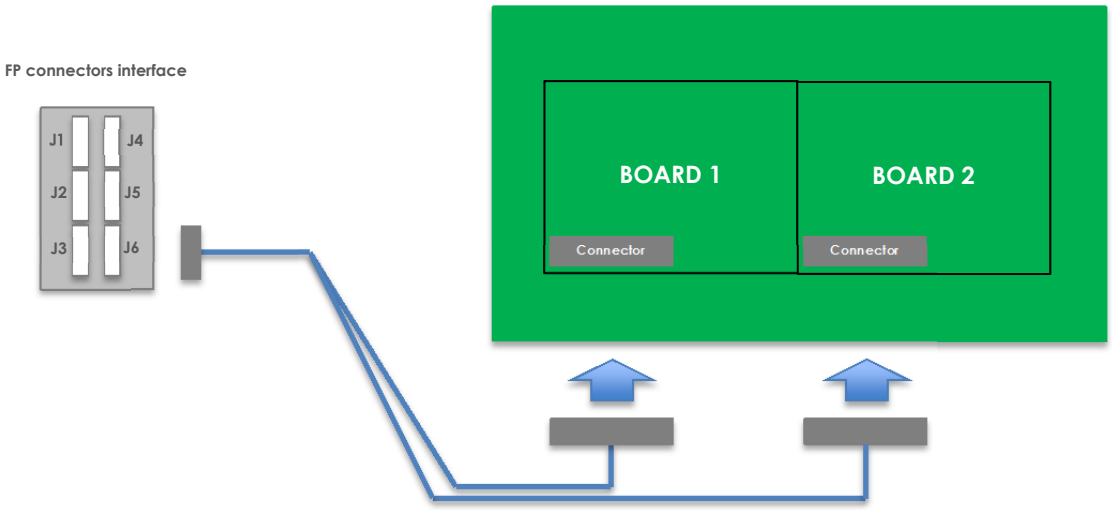


Fig. 1.6.2.a – Example of setup through cable on a panel of boards.

When arranging a setup as shown in Fig. 1.6.2.a, it is recommended to place the connectors of the external cable according to the following rules:

1) On the side with less or none accessibility to the copper tracks (so that the test with FP probes is executed on the opposite side).
2) As close as possible to the border of the UUT, in order to avoid the passage of the cable over the components (if the connector is on the same side used for the test).

The table below reports the applicability of the solution with cabling on panel of boards sorted by model of system:

	Shuttle Loader	Manual	In-Line	Back Panel
Applicability of cabling on panel of boards	•	•	• (1)	• (1)

(1) RSL (Removable Shuttle Loader) required if available on system tester.

€ Setup through cabling is usually less expensive than a fixture.

2. Specific aspects of board design

This chapter deals with specific aspect on the design of the board according to the typology of tests to execute.

2.1. Circuit configurations

An electronic board can encompass particular circuit functions which, when designed under ideal condition, can influence the coverage of the test program developed on FP.
The suggestions in the following chapters point to define an ideal route to making the board suitable not only for classic In-Circuit test, but also for functional test, devices programming, power-on tests etc.

2.1.1. Initialization circuits and electrical constraints

Some signals of the board under test may need to reach a specific state during a specific kind of electric test.
This state can be critical for their functioning and may be generically set up before starting the specific kind of test (In-Circuit, functional, programming etc).

Examples of typical initialization circuits or electrical constraints:

1) Reset circuits
2) Constraints between grounds or power supplies
3) Active high constraints
4) Active low constraints

The table below reports the applicable solutions to fulfill the electrical constraints during the test.

	Shuttle Loader 4 probes	**Manual 4 Probes**	**Manual 6 Probes**	**In-Line 4 Probes**	**In-Line 6 Probes**	**Back Panel 4 Probes**	**Back Panel 6 Probes**
Side of test	Top	Top	Top/Bottom	Top	Top/Bottom	Top	Top/Bottom
Ideal accessible side for the initialization/constraint points	Bottom/ Connector	Bottom/ Connector	Bottom/ Connector	Bottom/ Connector	Bottom/ Connector	Bottom/ Connector	Bottom/ Connector
How to initialize or constrain the signals							
Bottom side moving head	-	-	•	-	•	-	•
Cable	•	•	(1) (2)	(1) (2)	(1) (2)	(1) (2)	(1) (2)
Fixed probes	•	•	(2)	•	(2)	•	(2)
Fixture	•	•	(2)	•	(2)	•	(2)

(1) RSL (Removable Shuttle Loader) without plane required. RSL system availability required.
(2) RSL (Removable Shuttle Loader) with plane required. RSL system availability required.

Arranging the ties as showed in top table and related to the system to be used, it simplified the design reducing the general cost.

2.1.2. Frequency measurements

The FP is able to execute frequency measurements through the probes thanks to the electronics mounted on the axes themselves. In measuring oscillation frequencies, it is helpful to arrange the board to be tested so that no external hardwares are necessary and the measurements are conducted in the best way possible.
The FP can be equipped with a **Prescaler**, able to measure frequencies up to 30MHz. Refer to the table and examples below for further details.

	Powered Oscillator	Quartz	Circuit Oscillation
Max measurable frequency without Prescaler	100KHz	100KHz	100KHz
Max measurable frequency with Prescaler	30MHz	30MHz	30MHz
Direct measure applicability (1)	•	-	•
Indirect measure applicability (2)	•	•	•
Power priority: of the board	3	2	2
Power priority: of the circuit	2	1	1
Power priority: of the component	1	-	-

(1) The **direct** measurement of a frequency is executed at the output of the component generating the frequency itself.
(2) The **indirect** measurement of a frequency is executed after the component generating the frequency, therefore on another component.

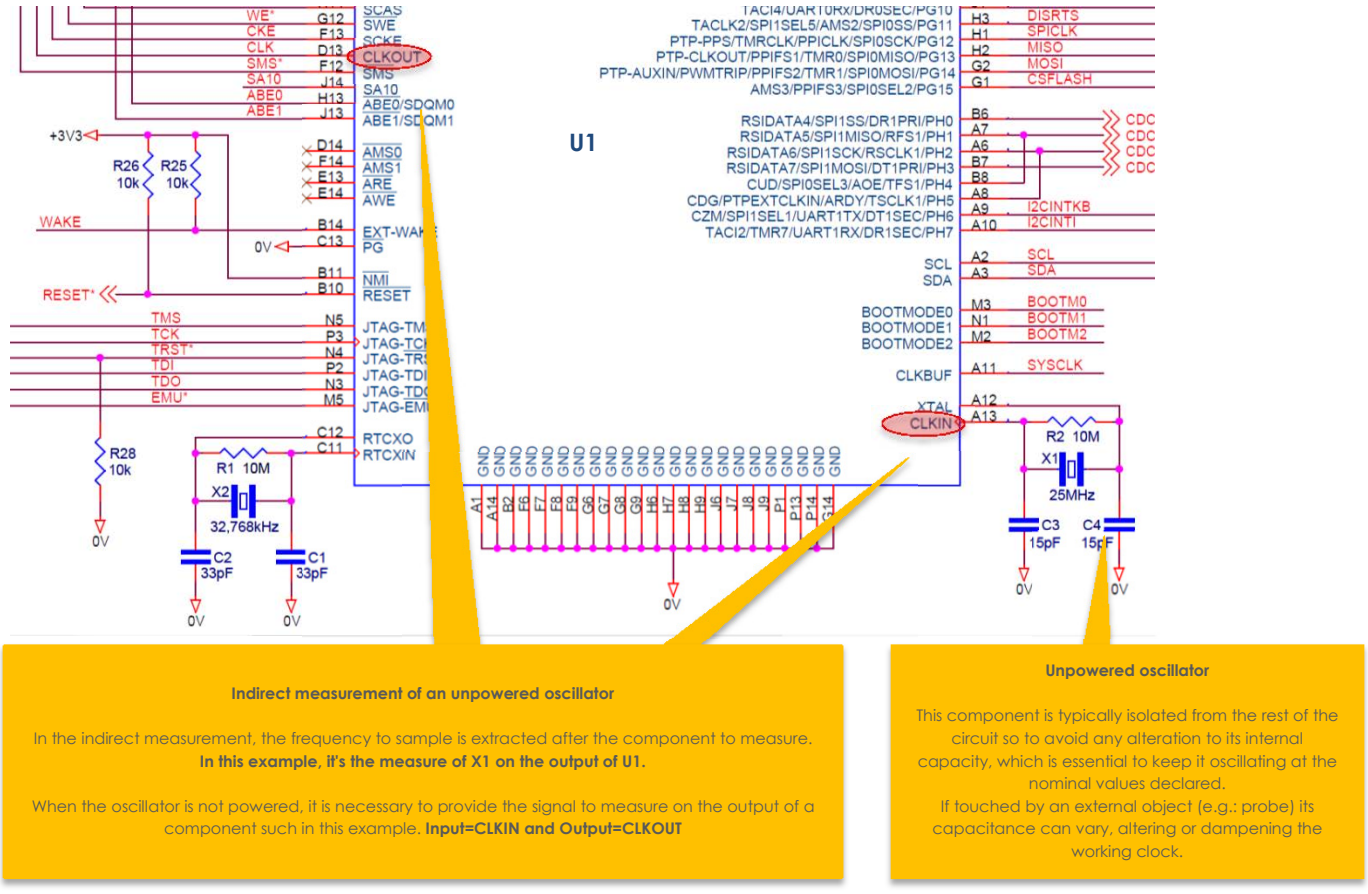


Fig. 2.1.2.a – Example of an indirect measurement of an unpowered oscillator.

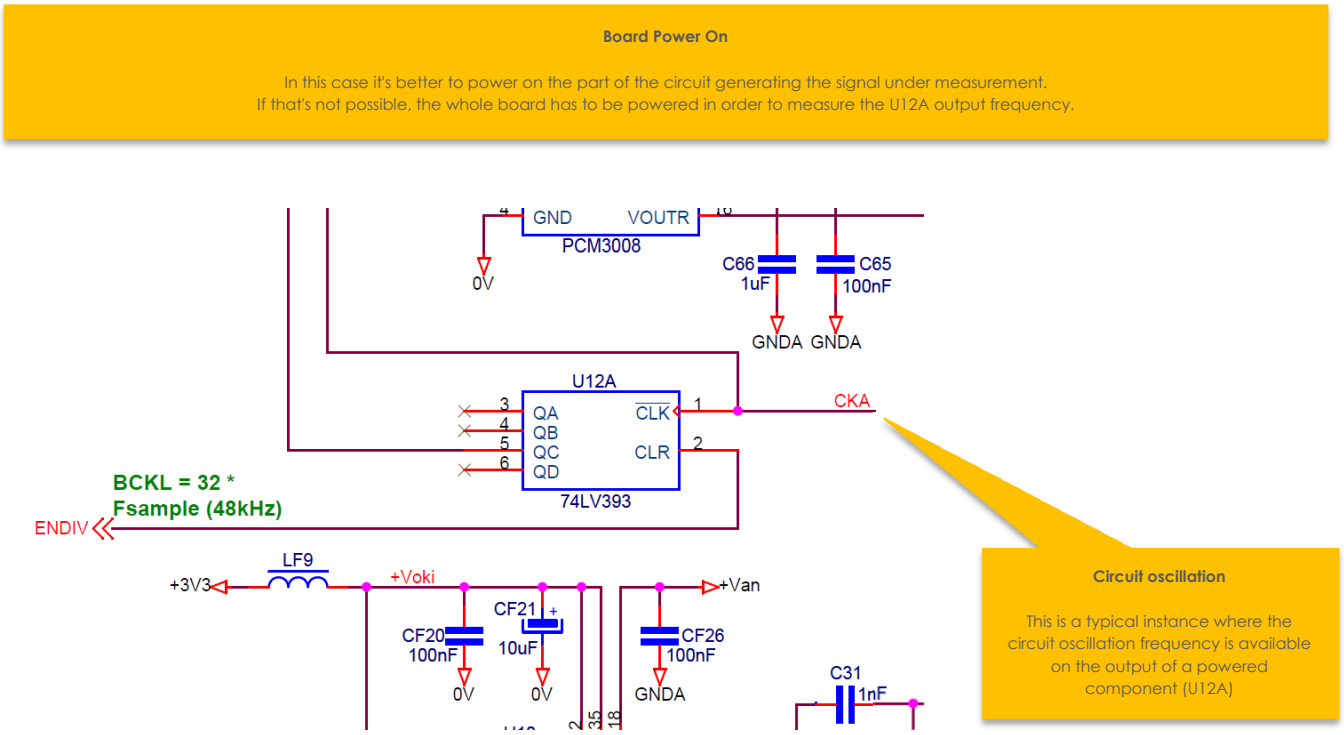
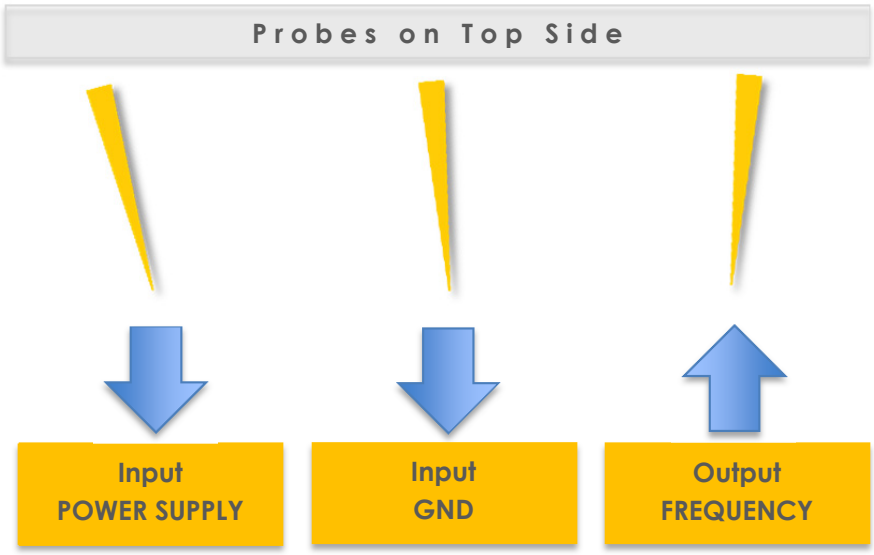


Fig. 2.1.2.b – Example an indirect measurement of the circuit oscillation

Arranging a pin on the output of a component to measure the clock of the board allows to increase the test coverage on FP, saving on the setup of an eventual functional test.

Designing all the necessary points to measure an oscillation (Power supply, GND and Output) on the same side of the board allows to simplify and speed up the implementation of a test in an FP program.

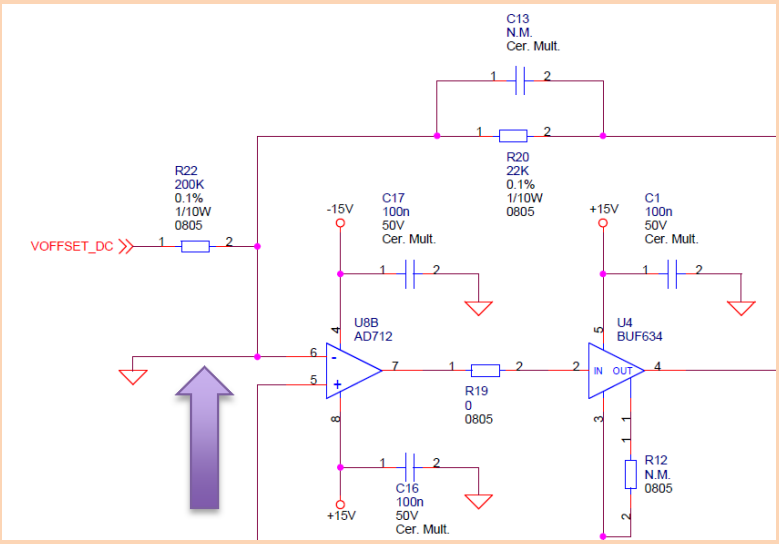


2.1.3. Designing for High and Low signal constraints

The FP test program can include Power On tests to verify the correct functioning of the analog and digital integrated circuits. On some of the pins of these components, the level of the signal can be constrained to high (es.: VCC) or low (es.: GND) due to electrical reasons. Fig. 2.1.3.a shows two methods to design Low signals constraints.

When aiming to increase the test coverage through the power on test, it's useful to arrange pull-up or pull-down resistors for the constrain of high and low signals, thus helping to enhance the test performance.

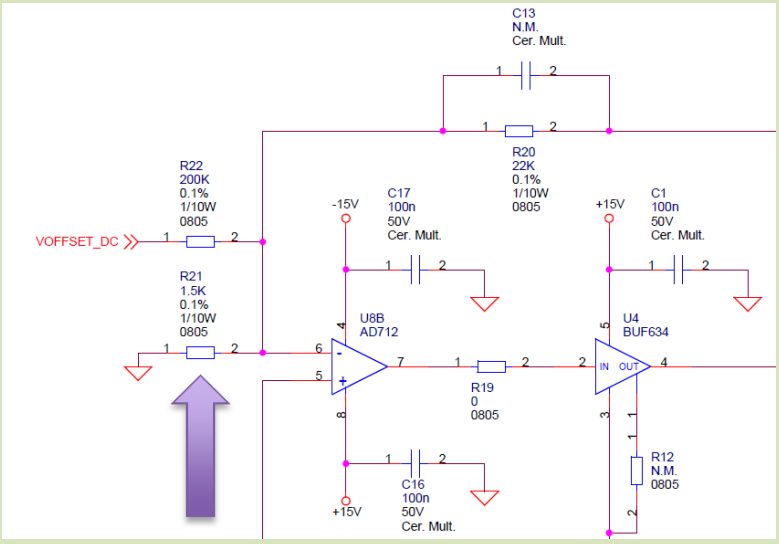
By designing pull-up and pull-down resistors to constrain signals to high or low, it's in fact possible to execute the power on tests by forcing all the inputs of the component to be tested (which would be impossible to do if the pin had been directly constrained through GND or VCC).



Non-ideal test condition

Pin 6 of component U8B directly constrained to GND

In this condition it is not possible to force pin 6 during the power on test, therefore the component will be **tested only partially.**



Ideal test condition

Pin 6 of component U8B connected to GND through pull-down

In this condition it is possible to force both pin 5 and pin 6 during the power on test, therefore the component will be completely tested.

Fig. 2.1.3.a – Example of design of a signal constrained to GND.

€ Designing pull-up or pull-down resistors increases the tests applicable to the integrated circuit, consequently improving its test coverage.

2.2. Removable Shuttle Loader (RSL)

The Removable Shuttle Loader, or RSL, is an instrument devised for In-Line systems and used for the following functions:

1) Transporting irregularly-shaped boards not prearranged for the in-line test
2) Transporting regularly-shaped boards not prearranged for the in-line test
3) Using external hardwares like cables and fixtures to enhance the test performance

Fig.2.2.a – RSL models

When using an In-Line system, the method used to transport the board to be tested has to be evaluated during the board designing. The table below summarizes, for each RSL model, the main characteristics to take into account:

	RSL 6xx	RSL 7xx
Maximum test area	300x440mm	300x440mm
Transport of irregularly-shaped boards not prearranged for the in-line test	•	•
Transport of regularly-shaped boards not prearranged for the in-line test	•	•
Support for pushing finger	•	-
Support for fixture	•	-
Support for cable	•	•
Accessibility to bottom probes	-	•
Connection to system interface	•	•

Fig.2.2.b – Example of a condition where the RSL is required

The RSL expands the versatility of the In-Line systems to test even boards not specifically designed to be tested with them or allowing to enhance the test performances through external hardwares (cable or fixture).

2.3. Components programming

The SPEA FP is able to program the components through a technique known as "On Board Programming" (or simply OBP). The integration of the OBP inside the Test Program is achieved using a dedicated, easy-to-use interface called SMART OBP.

The programming of the component can take place in three ways, according, typically, to the number of signals necessary for the programming:

1) Through FP probes
2) Through cable connected to the system interface
3) Through both (cable + probes)

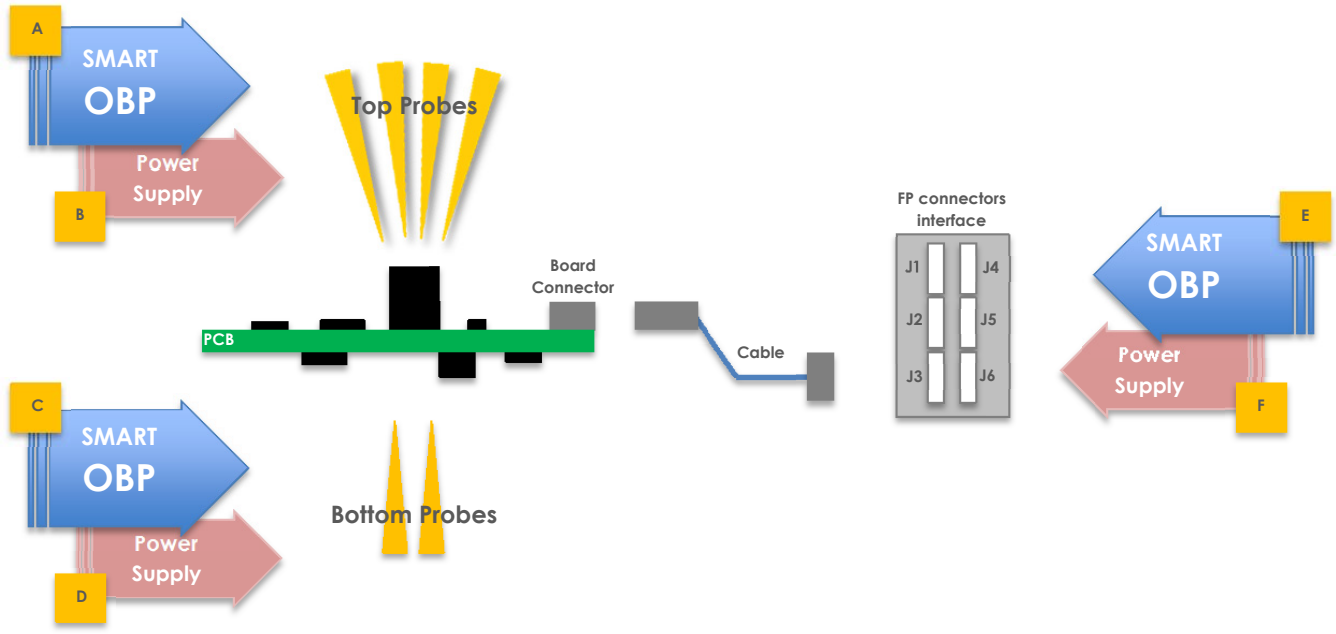


Fig. 2.3.a – Representation of the typical combinations used for the OBP

The following table shows the possible solutions pertaining OBP linked to the related costs and time for development.

	Programming signals	Component power supply	Combination required	Available Programming Signals	uC or board power supplies	Test Program Cost and Time of Development
Solution 1	Via Top Probes	Via Top Probes	A + B	2	2	- €
Solution 2	Via Top Probes	Via Bottom Probes	A + D	4	2	- €
Solution 3	Via Top and/or Bottom Probes	Via Cable	A + C + F	4 + 2	n	+ €
Solution 4	Via Cable	Via Cable	E + F	n	n	+ €

When designing the board to be tested on double-side contacting systems, arrange the accessibility of the power supplies component from the bottom and the programming signals from the top.

2.4. Open pin test

The SPEA FP is able to check the components pins welding through a 2 different techniques known as:

1. Electro scan
2. Junction scan

2.4.1. Electro scan

The test is based on empirical measurement acquisition of the pin under test. Below the test technique.

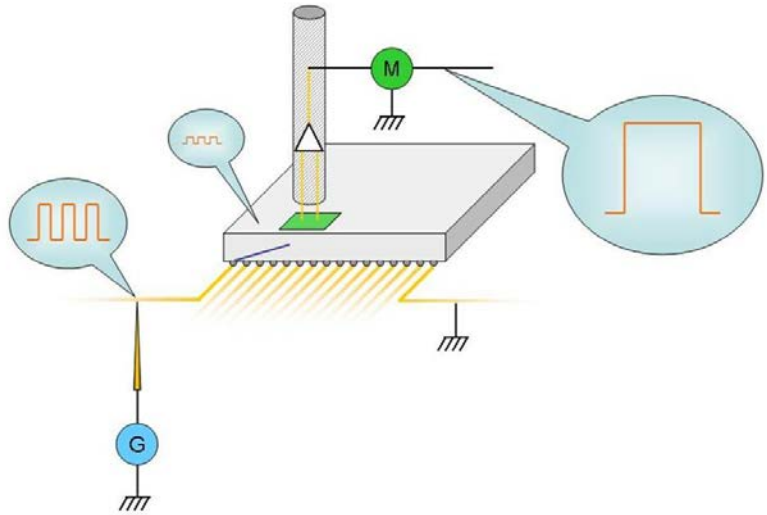


Fig.2.4.1.a – Test technique.

Respecting the parameters showed on following table will be possible to increase the performance of open pin test program reducing the debug time.

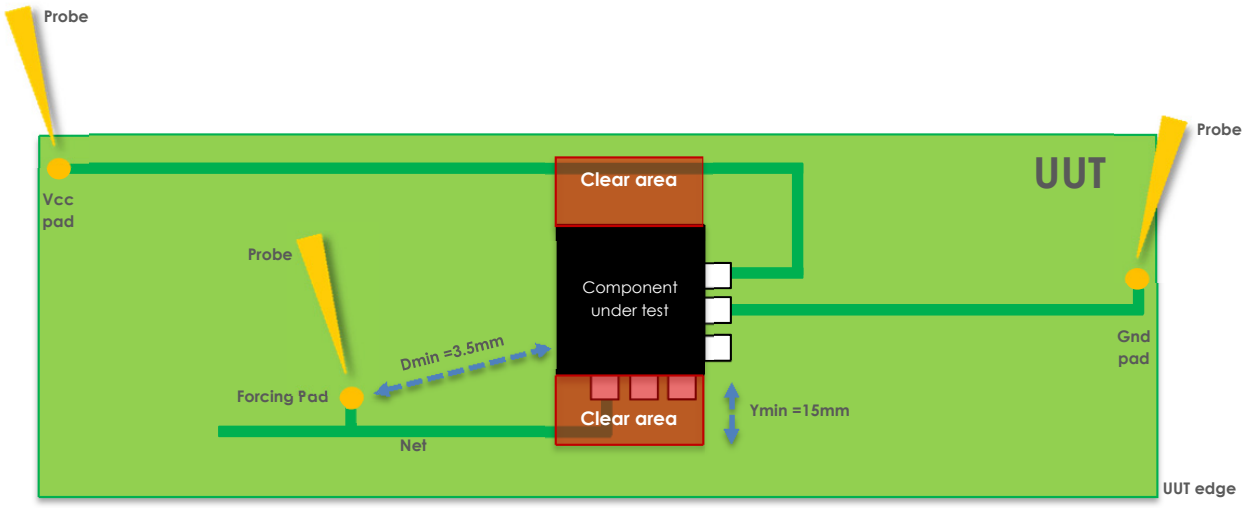


Fig.2.4.1.b – Board layout example.

	Value
Min. distance between the forcing pad to the case of the component (Dmin)	3.5 mm
Clear area suggested where the components height ≤ 7mm (Ymin)	15 mm
Component power net accessibility suggested	Close to the UUT edge
Component ground net accessibility suggested	Close to the UUT edge

2.5. Warping board

The warping issues can be solved using 4 different tools of the SPEA FP:

1. Manual contrast finger.
2. Automatic contrast finger.
3. Tray or fixture.
4. Warpage tool performed by specific laser.

Anyway the warping error can be considered during the design of the board pads following the example below:

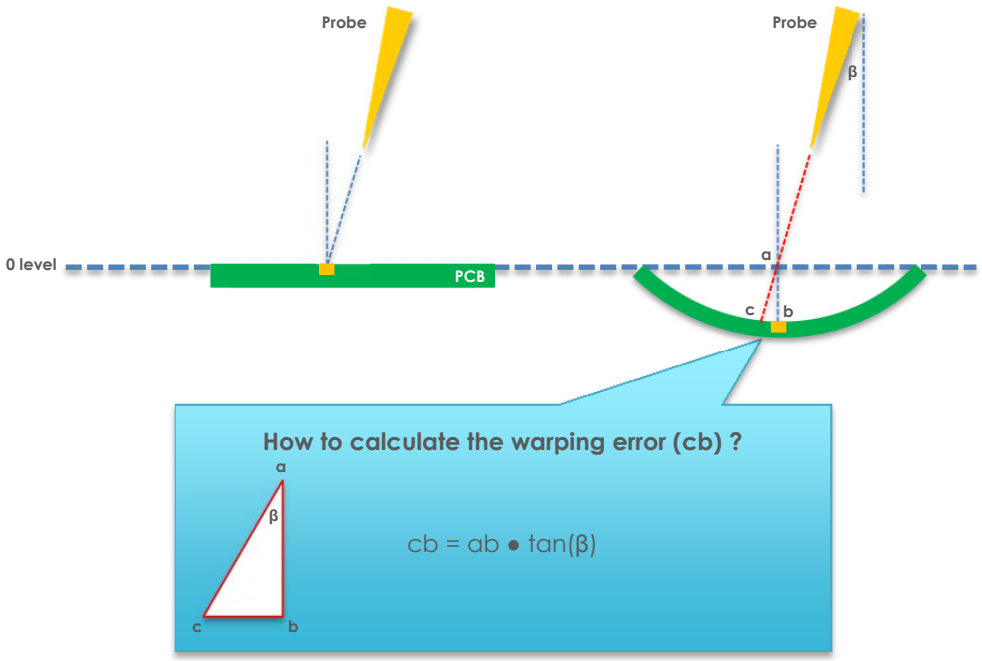


Fig. 2.5.a – Warping error calculation.

Design the UUT in order to simplify the use of contrast method available on own system.